In the Specification

Please amend the specification of this application as follows:

Rewrite the paragraph [0004] at page X, lines Y to Z as follows:

--[0004] Full adders (1)-(4) take 1-bit carry signal c_t of from the lower position as input, and at the same time, have 1-bit signals a and b as addition objects as inputs. Then, each of ~~said~~ the full adders outputs 1-bit signal s as the addition result, and at the same time, outputs 1-bit carry signal c_0 to the upper position. Addition result signal s and carry signal c_0 are expressed by the following equations, respectively.

[Numerical formula 1]

$$s = a \oplus b \oplus c_t \quad \cdots (1)$$

$$c_0 = a \cdot b + (a \oplus b) \cdot c_t \quad \cdots (2)$$

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Rewrite paragraph [0006] as follows:

--[0006] In the adder with the constitution shown in Figure 16A, before output of lower-position carry signal c_2, the addition result s_3 of the most significant position and its overflow signal c_3 are not determined. Also, ~~said~~ the carry signal c_2 is not determined until output of the lower-position carry signal c_1, and carry signal c_1 is not determined until output of the lower-position carry signal c_0.--

Rewrite paragraph [0007] as follows:

--[0007] That is, in order to determine the addition result and carry for a certain position, it is necessary to determine

the carry signals of all the positions lower than ~~said~~ the position. Consequently, the propagation path of the carry signal (indicated by broken line in Figure 16A) becomes the longest delay path (critical path) in the ripple type adder. As the bit length of the addition object signals increases, the number of stages of full adders that have to be added increases. All these added full adders are added to the critical path. Consequently, the delay time before the final addition result can be determined increases.--

Rewrite paragraph [0013] as follows:

--[0013] ~~Said~~ The 4-input NAND gate (9) takes carry generation signal g_0 from half adder (5) and carry propagation signals p_1 - p_3 output from half adders (6)-(8) as inputs, and outputs NAND of ~~said~~ the four input signals. This output signal corresponds to the NOT signal of the first item on the right side of Equation (6). ~~Said~~ The 3-input NAND gate (10) takes carry generation signal g_1 from half adder (6) and carry propagation signals p_2 and p_3 output from half adders (7) and (8) as inputs, and outputs NAND of ~~said~~ the three input signals. This output signal corresponds to the NOT signal of the second item on the right side of Equation (6). ~~Said~~ The 2-input NAND gate (11) takes carry generation signal g_2 from half adder (7) and carry propagation signal p_3 output from half adder (8) as inputs, and outputs NAND of ~~said~~ the two input signals. This output signal corresponds to the NOT signal of the third item on the right side of Equation (6). Inverter (12) outputs NOT of carry generation signal g_3 output from half adder (8). This output signal corresponds to the signal of NOT of the fourth item on the right side of Equation (6). ~~Said~~ The 4-input NAND gate (13) takes the output signals of NAND gates (9)-(11) and inverter (12) as its

inputs, and outputs NAND of the input four signals. This output signal corresponds to carry signal c_3 shown in Equation (6).--

Rewrite paragraph [0014] as follows:

--[0014] With the aid of ~~said~~ the generation circuit of carry signal c_3 with the constitution, carry signal c_3 can be formed directly from addition object signals ($a_0, \ldots, a_3$) and ($b_0, \ldots, b_3$), without waiting for determination of the lower-position carry signals (c_0 - c_2). Compared with the ripple carry system shown in Figure 16A, the delay in propagation of the carry signal can be shortened. The circuit shown in Figure 17A is a circuit for forming the carry signal for the 4th position counted from the least significant position. When a carry signal is to be formed for addition of more bits, one usually adopts a system in which plural CLA circuits are connected in a hierarchical constitution.--

Rewrite paragraph [0017] as follows:

--[0017] Figure 19 is a circuit diagram illustrating an example of constitution of 4-bit half adder (21). For example, as shown in Figure 19, ~~said~~ the 4-bit half adder (21) is composed of four half adders (30)-(33) of 1-bit half adders. Also, other 4-bit half adders (22)-(24) may have the same constitution as that shown in Figure 19. CLA circuits (25)-(28) have carry propagation 4-bit signals and carry generation 4-bit signals output from 4-bit half adders (21)-(24) as inputs, respectively, and , corresponding to these signals, they output carry propagation 1-bit signals and carry generation 1-bit signals, respectively.--

Rewrite paragraph [0018] as follows:

--[0018] That is, CLA circuit (25) has carry propagation signal (p_0, … p_3) and carry generation signal (g_0,..., g_3) of half adder (21) input to it. CLA circuit (26) has carry propagation signal (p_4, … p_7) and carry generation signal (g_4,..., g_7) of half adder (22) input to it. CLA circuit (27) has carry propagation signal (p_8, … p_{11}) and carry generation signal (g_8,..., g_{11}) of half adder (23) input to it. CLA circuit (28) has carry propagation signal (p_{12}, … p_{15}) and carry generation signal (g_{12},..., g_{15}) of half adder (24) input to it. Then, corresponding to ~~said~~ the inputs, carry propagation 1-bit signals and carry generation 1-bit signals are calculated. That is, CLA circuit (25) calculates and outputs carry propagation signal P_0 and carry generation signal G_0. CLA circuit (26) calculates and outputs carry propagation signal P_1 and carry generation signal G_1. CLA circuit (27) calculates and outputs carry propagation signal P_2 and carry generation signal G_2. CLA circuit (28) calculates and outputs carry propagation signal P_3 and carry generation signal G_3. The input carry propagation 4-bit signals for CLA circuits (25)-(28) are represented as signals $p_{(0)}$ - $p_{(3)}$ from the lower position, also, the input carry generation 4-bit signals are represented as signals $g_{(0)}$ - $g_{(3)}$. In this case, output 1-bit carry propagation signal P and output 1-bit carry generation signal G are expressed by the following equations.

[Numerical formula]

$$
\begin{aligned}
G = {} & p_{(3)} \cdot p_{(2)} \cdot p_{(1)} \cdot g_{(0)} \\
& + p_{(3)} \cdot p_{(2)} \cdot g_{(1)} \\
& + p_{(3)} \cdot g_{(2)} \\
& + g_{(3)} \quad \cdots (7)
\end{aligned}
$$

$$
P = p_{(3)} \cdot p_{(2)} \cdot p_{(1)} \cdot p_{(0)} \quad \cdots (8)
$$

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Rewrite paragraph [0020] as follows:

--[0020] In the generation circuit of carry signal c_{15} with the constitution, when i=15 in ~~said~~ the Equation (3), output carry generation signal Go of CLA circuit (29) is equal to carry signal c_{15}. That is, using Equation (3), carry signal c_{15} is expressed by the following equation.

[Numerical formula 7]

$$
\begin{aligned}
C_{15} = {} & p_{15} \cdot p_{14} \cdot \cdots \cdot p_1 \cdot g_0 \\
& + p_{15} \cdot p_{14} \cdot \cdots \cdot p_2 \cdot g_1 \\
& + p_{15} \cdot g_{14} \\
& + g_{15} \quad \cdots (9)
\end{aligned}
$$

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Rewrite paragraph [0028] as follows:

--[0028] Figure 5 in Japanese Kokai Patent Application No. Hei 5[1993]-61643 is a circuit diagram illustrating an example in which composite gates are used in a CLA circuit that generates the same signal as that of output carry generation signal G expressed by Equation (7). FIGURE 21 is a circuit diagram

illustrating an example of a CLA circuit made of ~~said~~ the composite gates. For the composite gate shown in FIGURE 21, four transistors, that is, p-type MOS transistors Qp1 - Qp4, are inserted in series between the input terminal of inverter (34) and power source line V_{CC}, and four transistors, that is, n-type MOS transistors Qn1 - Qn4, are inserted in series between the input terminal of inverter (34) and ground line G. Consequently, in order to increase the speed of the CLA circuit, it is necessary to increase the size of these transistors, and as explained above, problems of increase in circuit size and power consumption occur. This is undesirable.--

Rewrite paragraph [0032] as follows:

--[0032] A further aspect of this invention provides a carry look-ahead circuit having the carry look-ahead circuit output a carry generation signal corresponding to the result of OR operation from the first logic operation item to the Nth logic operation item for the (k - 1)th logic operation item and Nth logic operation item; here, the (k - 1)th logic operation item is equal to AND of the various positions from the Nth position to the kth position (where k is a natural number in the range of 2-N) of the input carry propagation signal and the (k - 1)th position of ~~said~~ the input carry generation signal, with the least significant position of the input (N - 1)-bit carry propagation signal (where N is a natural number) taken as the second position and the least significant position of the N-bit carry generation signal taken as the first position, and the Nth logic operation item is equal to the Nth position of ~~said~~ the output carry generation signal; the carry look-ahead circuit has the following logic gates: one or several first logic gates that perform the following operation: in the OR operation formula of N items with ~~said~~ the first logic operation item through Nth

logic operation item set side-by-side, grouping is performed with OR for every two adjacent items taken as a group item in the order from the side of ~~said~~ the first logic operation item to the side of ~~said~~ the Nth logic operation item; when a common item exists in the two grouped items, OR of the two items in ~~said~~ the group item is transformed to AND of ~~said~~ the common item and non-common item; when the number of ~~said~~ the group items in the OR operation formula after ~~said~~ the grouping is larger than 2, ~~said~~ the grouping and ~~said~~ the transformation are carried out repeatedly for ~~said~~ the group items in the order corresponding to ~~said~~ the number order in the OR operation formula after ~~said~~ the grouping; the OR operation formula made of two ~~said~~ the group items obtained in the above process is taken as the first logic formula; among the signals corresponding to AND, NAND, OR or NOR of ~~said~~ the input carry propagation signals of plural bits, ~~said~~ the input carry propagation signal, and ~~said~~ the input carry generation signal, 2-bit signals are input, and AND, NAND, OR or NOR of the input 2-bit signals is output from ~~said~~ the one or several first logic gates; and one or several second logic gates that perform the following operation: among the signals corresponding to the operation result for ~~said~~ the group item, ~~said~~ the common item, and ~~said~~ the non-common item in ~~said~~ the first logic formula, as well as ~~said~~ the input carry generation signal, ~~said~~ the input carry propagation signal, and the output signal of ~~said~~ the first logic gates, 3-bit signals are input; among the input signals, the signal corresponding to OR or NOR of AND of the 2-bit signals and the other 1-bit signal, or the signal corresponding to AND or NAND of OR of the 2-bit signals among the input signals and the other 1-bit signal is output as the signal corresponding to the operation result (or its NOT) for ~~said~~ the group item, ~~said~~ the non-common item, or ~~said~~ the output carry generation signal; The position that is one position lower

than the second position of ~~said~~ the input carry propagation signal is taken as the first position; ~~said~~ the first logic gate may also contain a logic gate that has the signal of the first position of ~~said~~ the input carry propagation signal input to it as a 1-bit signal among the input 2-bit signals, and a logic gate that outputs the carry propagation signal (or its NOT) corresponding to the result of operation for AND for the various positions from the first position to the Nth position of ~~said~~ the input carry propagation signal. Also, it may contain one or several third logic gates which take a 1-bit signal among ~~said~~ the input carry generation signal, ~~said~~ the input carry propagation signal, the output signal of ~~said~~ the first logic gate, and the output signal of ~~said~~ the second logic gate as input, perform NOT for ~~said~~ the input signal, and output the result to ~~said~~ the first logic gate or ~~said~~ the second logic gate, or which output [same] as ~~said~~ the output carry propagation signal or ~~said~~ the output carry generation signal.--

Rewrite paragraph [0033] as follows:

--[0033] Another aspect this invention provides an adder having the following circuits: a first logic operation circuit, which outputs exclusive OR of the various positions of two addition object signals as the carry propagation signal, and which outputs AND of the various positions of ~~said~~ the two addition object signals as the carry generation signal; a second logic operation circuit, which performs a carry operation for each position generated due to addition of ~~said~~ the addition object signals corresponding to ~~said~~ the carry propagation signal and ~~said~~ the carry generation signal of ~~said~~ the first logic operation circuit, and which outputs the operation result as the carry signal; and a third logic operation circuit, which performs exclusive OR for ~~said~~ the carry signal from the lower position

with respect to each position of ~~said~~ the addition object signal and ~~said~~ the carry propagation signal for each position, and which outputs the operation result as the result of addition of each position; ~~said~~ the second logic operation circuit contains one or several carry look-ahead circuits, which take ~~said~~ the carry propagation signals of plural bits and ~~said~~ the carry generation signals of plural bits output from ~~said~~ the first logic operation circuit as input, and which outputs an output carry propagation 1-bit signal and an output carry generation 1-bit signal, and a carry signal output circuit that outputs ~~said~~ the carry signal corresponding to ~~said~~ the carry propagation signal and ~~said~~ the carry generation signal of ~~said~~ the first logic operation circuit as well as ~~said~~ the output carry propagation signal and ~~said~~ the output carry generation signal of ~~said~~ the carry look-ahead circuit; ~~said~~ the carry look-ahead circuit comprises the carry look-ahead circuit outputs ~~said~~ the output carry generation signal corresponding to the result of OR operation from the first logic operation item to the Nth logic operation item for the (k - 1)th logic operation item and Nth logic operation item; here, the (k - 1)th logic operation item is equal to AND of the various positions from the Nth position to the kth position (where k is a natural number in the range of 2-N) of the input carry propagation signal and the (k - 1)th position of ~~said~~ the input carry generation signal; with the least significant position of ~~said~~ the N-bit carry propagation signal (where N is a natural number) input from ~~said~~ the first logic operation circuit and the least significant position of ~~said~~ the N-bit carry generation signal as the first positions, respectively, and the carry look-ahead circuit outputs ~~said~~ the output carry propagation signal corresponding to the result of operation for AND of the various positions from the first position to the Nth position of ~~said~~ the input carry propagation

signal; the carry look-ahead circuit has the following logic gates: one or several first logic gates that perform the following operation: in the OR operation formula of N items with ~~said~~ the first logic operation item through Nth logic operation item set side-by-side, grouping is performed with OR for every two adjacent items taken as a group item in the order from the side of ~~said~~ the first logic operation item to the side of ~~said~~ the Nth logic operation item; when a common item exists in the two grouped items, OR of the two items in ~~said~~ the group item is transformed to AND of ~~said~~ the common item and non-common item; when the number of ~~said~~ the group items in the OR operation formula after ~~said~~ the grouping is larger than 2, ~~said~~ the grouping and ~~said~~ the transformation are carried out repeatedly for ~~said~~ the group items in the order corresponding to ~~said~~ the number order in the OR operation formula after ~~said~~ the grouping; the OR operation formula made of two ~~said~~ the group items obtained in the above process is taken as the first logic formula; among the signals corresponding to AND, NAND, OR or NOR of ~~said~~ the input carry propagation signals of plural bits, ~~said~~ the input carry propagation signal, and ~~said~~ the input carry generation signal, 2-bit signals are input, and AND, NAND, OR or NOR of the input 2-bit signals is output from ~~said~~ the one or several first logic gates; and one or several second logic gates that perform the following operation: among the signals corresponding to the operation result of ~~said~~ the group item, ~~said~~ the common item, and ~~said~~ the non-common item in ~~said~~ the first logic formula, as well as ~~said~~ the input carry generation signal, ~~said~~ the input carry propagation signal, and the output signal of ~~said~~ the first logic gates, 3-bit signals are input; among the input signals, the signal corresponding to OR or NOR of AND of 2-bit signals and the other 1-bit signal, or the signal corresponding to AND or NAND of OR of 2-bit signals among the

input signals and the other 1-bit signal is output as the signal corresponding to the operation result (or its NOT) of ~~said~~ the group item, ~~said~~ the non-common item, or ~~said~~ the output carry generation signal.--

Rewrite paragraph [0036] as follows:

--[0036] In the following, a 4-bit CLA circuit pertaining to Embodiment 1 of this invention will be explained. The 4-bit CLA circuit has the 4-bit carry propagation signal (p_0,…, p_3) and 4-bit carry generation signal (g_0,…, g_3) as inputs, and, corresponding to ~~said~~ the input signals, it outputs 1-bit carry propagation signal P and 1-bit carry generation signal G. The least significant position (the first position),…, and the most significant position (the fourth position) of the 4-bit carry propagation signal correspond to carry propagation signals p_0,…, p_3, respectively. Also, the least significant position (the first position),..., and the most significant position (the fourth position) of the 4-bit carry generation signal correspond to carry generation signals g_0,…, g_3, respectively. Using carry propagation signal (p_0,..., p_3) and carry generation signal (g_0,…, g_3), carry propagation signal P and carry generation signal G can be expressed by the following equations.

[Numerical formula 12]

$$G = p_3 \cdot p_2 \cdot p_1 \cdot g_0 + p_3 \cdot p_2 \cdot g_1 + p_3 \cdot g_2 + g_3 \quad \cdots \text{(14)}$$
$$P = p_3 \cdot p_2 \cdot p_1 \cdot p_0 \quad \cdots \text{(15)}$$

--

Rewrite paragraph [0037] as follows:

--[0037] If AND of the fourth position to second position of the input carry propagation signal and the first position of

the input carry generation signal is taken as the first logic operation item, this first logic operation item corresponds to the first item ($p_3 \cdot p_2 \cdot p_1 \cdot g_0$) on the right side of Equation (14). If AND of the fourth position to third position of the input carry propagation signal and the second position of the input carry generation signal is taken as the second logic operation item, this second logic operation item corresponds to the second item ($p_3 \cdot p_2 \cdot g_1$) on the right side of Equation (14). If AND of the fourth position of the input carry propagation signal and the third position of the input carry generation signal is taken as the third logic operation item, this third logic operation item corresponds to the third item ($p_3 \cdot g_2$) on the right side of Equation (14). If the fourth position of the input carry generation signal is taken as the fourth logic operation item, this fourth logic operation item corresponds to the fourth item (g_3) on the right side of Equation (14). Consequently, carry generation signal G output from the 4-bit CLA circuit is given as a result of the operation of OR of ~~said~~ the four items (first logic operation item - fourth logic operation item).--

Rewrite paragraph [0038] as follows:

--[0038] Here, for ~~said~~ the Equation (14), the following transformation is performed. Equation (14) is a formula of operation of OR of the four items, that is, ~~said~~ the first logic operation item through the fourth logic operation item set side-by-side in numerical order. First of all, for ~~said~~ the Equation (14), grouping is performed with OR for every adjacent two items taken as a group item in the order from the first logic operation item or the fourth logic operation item, that is, from the left side or right side of the equation in a sequential way. Then, when a common item exists in the two grouped items, OR of

the two items in the group items is transformed to AND of the common item and non-common item.--

Rewrite paragraph [0039] as follows:

--[0039] The following is the equation representing the operation of OR after ~~said~~ the grouping and transformation.

[Numerical formula 13]

$$G = (p_3 \cdot p_2) \cdot (p_1 \cdot g_0 + g_1) + (p_3 \cdot g_2 + g_3) \quad \cdots \text{(16)}$$

In Equation (16), the first and second items on the right side are ~~said~~ the group items, respectively. Among them, the first item on the right side is transformed to AND of common item $(p_3 \cdot p_2)$ and non-common item $(p_1 \cdot g_0 + g_1)$. When the number of group items in the OR operation formula after grouping is larger than 2, ~~said~~ the grouping and ~~said~~ the transformation are carried out repeatedly for ~~said~~ the group items in the order corresponding to ~~said~~ the number order of the first - fourth logic operation items in the OR operation formula after ~~said~~ the grouping. Because the number of group items is 2 for the OR operation formula of Equation (16), in this case, no further grouping and transformation are performed.--

Rewrite paragraph [0040] as follows:

--[0040] As far as the structure of Equation (16) obtained here is concerned, one can see that the generation circuit of carry generation signal G can be composed of two types of gates. That is, one can form the generation circuit of carry generation signal G shown in Equation (16) by using a gate (first logic gate) that outputs a signal corresponding to AND of input 2-bit

signals and a gate (second logic gate) that outputs a signal corresponding to OR of AND of 2-bit signals among input 3-bit signals and the other 1-bit signal. Also, the generation circuit of carry propagation signal P shown in Equation (15) can be composed of plural ~~said~~ the first logic gates. Consequently, the 4-bit CLA circuit can be formed from ~~said~~ the first logic gates and second logic gates.--

Rewrite paragraph [0041] as follows:

--[0041] Figure 1 is a circuit diagram illustrating an example of the constitution of the 4-bit CLA circuit in Embodiment 1 of this invention. The 4-bit CLA circuit shown in Figure 1 has NAND gates 101 and 102, NOR gate 103, AND-NOR type composite gates 201 and 202, and OR-NAND type composite gate 251. NAND gates 101 and 102 as well as NOR gate 103 form an embodiment of the first logic gate of this invention. AND-NOR composite gates 201 and 202 as well as OR-NAND type composite gate 251 form an embodiment of the second logic gate of this invention. NAND gate 101 has carry propagation signals p_0 and p_1 as its inputs, and outputs their NAND. NAND gate 102 takes carry propagation signals p_2 and p_3 as inputs, and outputs their NAND. The output signal corresponds to the signal of NOT of the result of operation for the common item ($p_3 \cdot p_2$) in Equation (16). NOR gate 103 outputs NOR of the output signals of NAND gates 101 and 102. This output signal corresponds to the result of operation for carry propagation signal P shown in Equation (15). Also, NOR of the two signals is equivalent to the result of AND after NOT of ~~said~~ the signals, respectively. In the example shown in FIGURE 1, in order to facilitate understanding, the symbols of NOR gates have been replaced with the symbols of the equivalent AND gates.--

Rewrite paragraph [0042] as follows:

--[0042] AND-NOR type composite gate 201 takes carry generation signals g_0 and g_1 as well as carry propagation signal p_1 as inputs, and it outputs NOR of the AND of carry propagation signal p_1 and carry generation signal g_0 and of carry generation signal g_1. This output signal corresponds to the signal of NOT of the result of operation for non-common item $(p_1 \cdot g_0 + g_1)$ in Equation (16). AND-NOR type composite gate 202 takes carry generation signals g_2 and g_3 as well as carry propagation signal p_3 as inputs, and it outputs NOR of the AND of carry propagation signal p_3 and carry generation signal g_2 and of carry generation signal g_3. This output signal corresponds to the signal of NOT of the result of operation for the group item $(p_3 \cdot g_2 + g_3)$ in Equation (16). OR-NAND type composite gate 251 outputs NAND of the OR of the output signals of NAND gate 102 and NAND-NOR type composite gate 201 and the output of AND-NOR type composite gate 202. This output signal corresponds to the result of operation for carry generation signal G shown in Equation (16). Also, AND of the OR of the two signals and the one signal is equal to OR of the result of the operation of AND of NOT of ~~said~~ <u>the</u> two signals and the result of NOT of ~~said~~ <u>the</u> one signal. In the example shown in FIGURE 1, in order to facilitate understanding, the symbol of the OR-NAND type composite gate is replaced with the symbol of AND-OR equivalent to it.--

Rewrite paragraph [0044] as follows:

--[0044] The AND-NOR type composite gate shown in FIGURE 2(C) has the same constitution as that shown in FIGURE 2(B). The two, however, are different from each other in the connection configuration of the parallel circuit of p-type MOS transistors Qp10 and Qp11 and p-type MOS transistor Qp12. That is, in the circuit shown in FIGURE 2(C), the parallel circuit of p-type MOS

transistors Qp10 and Qp11 is connected to output terminal Y, and p-type MOS transistor Qp12 is connected to power source line Vcc. On the other hand, in the circuit shown in FIGURE 2(B), connection is made reverse to ~~said~~ the configuration. However, although there is ~~said~~ the difference, the two are identical to each other with respect to operation pertaining to ON/OFF of conduction between power source line Vcc and output terminal Y. Consequently, in the circuit shown in FIGURE 2(C), also, the same function as that of the circuit shown in FIGURE 2(B) can be realized.--

Rewrite paragraph [0046] as follows:

--[0046] When input terminal C is on the high level and input terminal A and/or input terminal B are on the high level, n-type MOS transistor Qn15 is ON, and n-type MOS transistor Qn13 and/or Qn14 are ON. Consequently, output terminal Y and ground line G are connected to each other. Also, because p-type MOS transistor Qp15 is OFF and p-type MOS transistor Qp13 and/or Qp14 are OFF, connection between output terminal Y and power source line Vcc is cut off. Consequently, output terminal Y becomes low level. By means of ~~said~~ the operation, a signal corresponding to NAND of the OR of input terminals A and B and the input signal of input terminal C is output from output terminal Y.--

Rewrite paragraph [0047] as follows:

--[0047] The OR-NAND type composite gate shown in Figure 3(C) has the same constitution as that shown in FIGURE 3(B). The two, however, are different from each other with respect to the connection configuration of the parallel circuit of n-type MOS transistors Qn13 and Qn14 and n-type MOS transistor Qn15. That is, in the circuit shown in Figure 3(C), the parallel circuit of n-type MOS transistors Qn13 and Qn14 is connected to output

terminal Y, and n-type MOS transistor Qn15 is connected to ground line G. On the other hand, in the circuit shown in FIGURE 3(B), the connection is the reverse of ~~said~~ the configuration. However, although there is ~~said~~ the difference, the two are identical to each other with respect to operation pertaining to ON/OFF of conduction between ground line G and output terminal Y. Consequently, in the circuit shown in FIGURE 3(C), too, the same function as that of the circuit shown in FIGURE 3(B) can be realized.--

Rewrite paragraph [0049] as follows:

--[0049] As the first logic gates, NAND gates 101, 102 and NOR gate 103 are used, and, as the second logic gates, AND-NOR type composite gates 201, 202 and OR-NAND type composite gate 251 are used. For example, the second logic gate can be realized from the AND-NOR type composite gate shown in Figure 2 or the OR-NAND type composite gate shown in Figure 3. By using ~~said~~ the composite gates, the number of series stages of transistors inserted between output terminal Y and power source line Vcc and the number of series stages of transistors inserted between output terminal Y and ground line G are at most 2 stages. This stage number is the same as that of a 2-input NAND gate or 2-input NOR gate used in a conventional logic circuit.--

Rewrite paragraph [0056] as follows:

--[0056] Consequently, carry generation signal G output from the 5-bit CLA circuit is given as a result of the operation of OR of ~~said~~ the five items (first logic operation item - fifth logic operation item). Here, for ~~said~~ the Equation (17), just as in the case of Equation (16), the following transformation is performed. Equation (17) is a formula of operation of OR of the five items, that is, ~~said~~ the first logic operation item through

the fifth logic operation item, set side-by-side in numerical order. First of all, for ~~said~~ the Equation (17), grouping is performed with OR for every adjacent two items taken as a group item in order from the first logic operation item or the fifth logic operation item, that is, from the left side or right side of the equation in a sequential way. Then, when a common item exists in the two grouped items, OR of the two items in the group item is transformed to AND of the common item and non-common item--

Rewrite paragraph [0057] as follows:

--[0057] The following is the equation representing the operation of OR after ~~said~~ the grouping and transformation from the left side of Equation (17).

[Numerical formula 15]

$$G = (p_4 \cdot p_3 \cdot p_2) \cdot (p_1 \cdot g_0 + g_1) + p_4 (p_3 \cdot g_2 + g_3) + g_4 \quad \cdots (19)$$

In Equation (19), the first - third items on the right side are ~~said~~ the group items, respectively. Among them, the first item on the right side is transformed to AND of common item ($p_4 \cdot p_3 \cdot p_2$) and non-common item ($p_1 \cdot g_0 + g_1$). The second ~~tem~~ term on the right side is transformed to AND of common item (p_4) and non-common item ($p_3 \cdot g_2 + g_3$). Also, the third item on the right side (g_4) is the other item in the grouping treatment of Equation (17), and it is also handled as one group item. When the number of group items in the OR operation formula after grouping is larger than 2, ~~said~~ the grouping and ~~said~~ the transformation are carried out repeatedly for ~~said~~ the group items in the order corresponding to ~~said~~ the number order of the first - fifth logic operation items

in the OR operation formula after ~~said~~ the grouping. Because the number of group items is 3 for the OR operation formula of Equation (19), further grouping and transformation are performed.--

Rewrite paragraph [0058] as follows:

--[0058] When grouping and transformation are performed from the left side of Equation (19), the operation formula of OR of Equation (19) becomes the following equation.

[Numerical formula 16]

$$G = p_4\{(p_3 \cdot p_2) \cdot (p_1 \cdot g_0 + g_1) + (p_3 \cdot g_2 + g_3)\} + g_4 \quad \cdots (20)$$

Because the group item number is 2 for Equation (20), no further grouping and transformation are performed for Equation (20). As far as the structure of Equation (20) obtained here is concerned, one can see that the generation circuit of carry generation signal G can be composed of two types of gates. That is, one can form the generation circuit of carry generation signal G shown in Equation (20) by using ~~said~~ the first logic gate and second logic gate.--

Rewrite paragraph [0059] as follows:

--[0059] When a NAND gate or NOR gate is used as the first logic gate, or when an AND-NOR type composite gate and OR-NAND type composite gate is used the second logic gate, in addition to the first logic gate and second logic gate, it is necessary to have a third logic gate, that is, an inverter, that outputs NOT of a 1-bit signal. Also, for the generation circuit of carry propagation signal P shown in Equation (18), one may use plural

~~said~~ the first logic gates. Consequently, the 5-bit CLA circuit can be formed using two types of gates (first and second logic gates) or three types of gates (first logic gate - third logic gate).--

Rewrite paragraph [0063] as follows:

--[0063] In the following, a 5-bit CLA circuit pertaining to Embodiment 3 of this invention will be explained. ~~Said~~ The Equation (20) is a logic formula obtained by grouping the following three group items in Equation (19)

$(p_4 \cdot p_3 \cdot p_2) \cdot (p_1 \cdot g_0 + g_1)$,

$p_4 \cdot (p_3 \cdot g_2 + g_3)$,

g_4,

from the side of the first logic operation item, that is, from the left side of Equation (19). Then, in a reverse way, grouping and transformation are performed from the right side of Equation (19), and the following equation is obtained.

[Numerical formula 17]

$$G = (p_4 \cdot p_3 \cdot p_2) \cdot (p_1 \cdot g_0 + g_1) + \{p_4 (p_3 \cdot g_2 + g_3) + g_4\} \quad \cdots (21)$$

By studying the constitution of Equation (21) obtained in the above, one can see that a 5-bit CLA circuit with a constitution different from that of the circuit shown in Figure 4 can be formed using ~~said~~ the two types of gates (first and second logic gates) or three types of gates (first logic gate - third logic gate).--

Rewrite paragraph [0067] as follows:

--[0067] In the following, a 5-bit CLA circuit pertaining to Embodiment 4 of this invention will be explained. ~~Said~~ The Equation (19) is a logic formula obtained by grouping the following five group items in Equation (17) (first logic operation item - fifth logic operation item)

$p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot g_0$,

$p_4 \cdot p_3 \cdot p_2 \cdot g_1$,

$p_4 \cdot p_3 \cdot g_2$,

$p_4 \cdot g_3$,

g_4,

from the side of the first logic operation item, that is, from the left side of Equation (17). Then, in a reverse way, grouping and transformation are performed from the right side of Equation (17), and the following equation is obtained.

[Numerical formula 18]

$$G = p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot g_0 + (p_4 \cdot p_3) \cdot (p_2 \cdot g_1 + g_2) + (p_4 \cdot g_3 + g_4) \quad \cdots \quad (22)$$

Because the number of group items is 3 in Equation (22), further grouping and transformation are performed. When grouping and transformation are performed from the right side of Equation (22), the logic formula of Equation (22) becomes the following equation.

[Numerical formula 19]

$$G = p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot g_0 + \{(p_4 \cdot p_3) \cdot (p_2 \cdot g_1 + g_2) + (p_4 \cdot g_3 + g_4)\} \cdots (23)$$

By studying the constitution of Equation (23) obtained above, one can see that it is possible to form a 5-bit CLA circuit having a constitution different from that of the circuits shown in FIGS. 4 and 5 by using ~~said~~ <u>the</u> two types of gates (first and second logic gates) or three types of gates (first logic gate - third logic gate).--

Rewrite paragraph [0070] as follows:

--[0070] In the following, a 5-bit CLA circuit pertaining to Embodiment 5 of this invention will be explained. ~~Said~~ <u>The</u> Equation (23) is a logic formula obtained by grouping the following three group items in Equation (22)

$p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot g_0$,
$p_4 \cdot p_3 \cdot (p_2 \cdot g_1 + g_2)$,
$(p_4 \cdot g_3 + g_4)$

from the side of the first logic operation item, that is, from the right side of Equation (22). Then, in a reverse way, grouping is performed from the side of the 5th logic calculation item, that is, the left side of Equation (22), and the following equation is obtained.

[Numerical formula 20]

$$G = (p_4 \cdot p_3)\{p_2 \cdot p_1 \cdot g_0 + (p_2 \cdot g_1 + g_2)\} + (p_4 \cdot g_3 + g_4) \quad \cdots (24)$$

By studying the constitution of Equation (24) obtained above, one can see that it is possible to form a 5-bit CLA circuit having a constitution different from that of the circuits shown in FIGS. 4-6 by using ~~said~~ the two types of gates (first and second logic gates) or three types of gates (first logic gate - third logic gate).--

Rewrite paragraph [0073] as follows:

--[0073] In the following, a 6-bit CLA circuit pertaining to Embodiment 6 of this invention will be explained. The 6-bit CLA circuit has a 6-bit carry propagation signal (p_0,…, p_5) and 6-bit carry generation signal (g_0,…, g_5) as inputs, and, corresponding to ~~said~~ the input signals, it outputs 1-bit carry propagation signal P and 1-bit carry generation signal G. The least significant position (the first position),…, and the most significant position (the sixth position) of the 6-bit carry propagation signal correspond to carry propagation signals p_0,…, p_5, respectively. Also, the least significant position (the first position),..., and the most significant position (the sixth position) of the 6-bit carry generation signal correspond to carry generation signals g_0, …, g_5, respectively. Using carry propagation signal (p_0, ..., p_5) and carry generation signal (g_0,…, g_5), carry propagation signal P and carry generation signal G can be expressed by the following equations.

[Numerical formula 21]

$$G = p_5 \cdot p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot g_0 + p_5 \cdot p_4 \cdot p_3 \cdot p_2 \cdot g_1 + p_5 \cdot p_4 \cdot p_3 \cdot g_2 + p_5 \cdot p_4 \cdot g_3 + p_5 \cdot g_4 + g_5 \cdots (25)$$

$$P = p_5 \cdot p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot p_0 \cdots (26)$$

If AND of the sixth position to second position of the input carry propagation signal and the first position of the input carry generation signal is taken as the first logic operation item, this first logic operation item corresponds to the first item ($p_5 \cdot p_4 \cdot p_3 \cdot p_2 \cdot p_1 \cdot g_0$) on the right side of Equation (25). If AND of the sixth position to third position of the input carry propagation signal and the second position of the input carry generation signal is taken as the second logic operation item, this second logic operation item corresponds to the second item ($p_5 \cdot p_4 \cdot p_3 \cdot p_2 \cdot g_1$) on the right side of Equation (25). If AND of the sixth position to fourth position of the input carry propagation signal and the third position of the input carry generation signal is taken as the third logic operation item, this third logic operation item corresponds to the third item ($p_5 \cdot p_4 \cdot p_3 \cdot g_2$) on the right side of Equation (25). If AND of the sixth position to fifth position of the input carry propagation signal and the fourth position of the input carry generation signal is taken as the fourth logic operation item, this fourth logic operation item corresponds to the fourth item ($p_5 \cdot p_4 \cdot g_3$) on the right side of Equation (17). If AND of the sixth position of the input carry propagation signal and the fifth position of the input carry generation signal is taken as the fifth logic operation item, this fifth logic operation item corresponds to the fifth item ($p_5 \cdot g_4$) on the right side of Equation (25). If the sixth position of the input carry generation signal is taken as the sixth logic operation item, this sixth logic operation item corresponds to the sixth item (g_5) on the right side of

Equation (25). Consequently, carry generation signal G output from the 6-bit CLA circuit is given as a result of the operation of OR of ~~said~~ <u>the</u> six items (first logic operation item - sixth logic operation item). Here, for ~~said~~ <u>the</u> Equation (25), the following transformation is performed in the same way as for Equations (16), (19) and (22).--

Rewrite paragraph [0074] as follows:

--[0074] Equation (25) is a formula of operation of OR of six items, that is, ~~said~~ <u>the</u> first logic operation item through the sixth logic operation item set side-by-side in numerical order. First of all, for ~~said~~ <u>the</u> Equation (25), grouping is performed with OR of every adjacent two items taken as a group item in order from the first logic operation item or the sixth logic operation item, that is, from the left side or right side of the equation in a sequential way. Then, when a common item exists in the two group items, OR of the two items in the group item is transformed to AND of the common item and non-common item. The following is the equation representing the operation of OR of Equation (25) after ~~said~~ <u>the</u> grouping and transformation from the left side or right side of Equation (25).

[Numerical formula 22]

$$G = (p_5 \cdot p_4 \cdot p_3 \cdot p_2)(p_1 \cdot g_0 + g_1) + (p_5 \cdot p_4) \cdot (p_3 \cdot g_2 + g_3) + (p_5 \cdot g_4 + g_5) \quad \cdots (27)$$

In Equation (27), the first - third items on the right side are ~~said~~ <u>the</u> group items, respectively. Among them, the first item on the right side is transformed to AND of common item ($p_5 \cdot p_4 \cdot p_3 \cdot p_2$) and non-common item ($p_1 \cdot g_0 + g_1$), and the second item on the right side is transformed to AND of common item ($p_5 \cdot p_4$) and non-common

item ($p_3 \cdot g_2 + g_3$). Because the number of group items is 3 for the group items in Equation (27), in this case, further grouping and transformation are performed. As grouping and transformation are further performed from the left side of Equation (27), Equation (27) becomes the following equation.

[Numerical formula 23]

$$G = (p_5 \cdot p_4)\{(p_3 \cdot p_2)(p_1 \cdot g_0 + g_1) + (p_3 \cdot g_2 + g_3)\} + (p_5 \cdot g_4 + g_5) \quad \cdots (28)$$

Because the number of group items in equation (28) is 2 for the grouped items in Equation (28), in this case, no further grouping and transformation are performed.--

Rewrite paragraph [0075] as follows:

--[0075] As far as the structure of Equation (28) obtained here is concerned, one can see that the generation circuit of carry generation signal G can be composed of ~~said~~ the two types of gates (first logic gate and second logic gate), or three types of gates (first logic gate - third logic gate). Also, the generation circuit of carry propagation signal P shown in Equation (26) can be composed of plural ~~said~~ the first logic gates. Consequently, the 6-bit CLA circuit can be formed from ~~said~~ the two types of gates (first logic gate and second logic gate), or three types of gates (first logic gate - third logic gate).--

Rewrite paragraph [0078] as follows:

--[0078] In the following, a 6-bit CLA circuit pertaining to Embodiment 7 of this invention will be explained. ~~Said~~ The

Equation (28) is a logic formula obtained by grouping the following three group items in Equation (27)

$(p_5 \cdot p_4 \cdot p_3 \cdot p_2) \cdot (p_1 \cdot g_0 + g_1)$、

$(p_5 \cdot p_4) \cdot (p_3 \cdot g_2 + g_3)$、

$(p_5 \cdot g_4 + g_5)$,

from the side of the first logic operation item, that is, from the left side of Equation (27). Then, in a reverse way, grouping and transformation are performed from the right side of Equation (27), and the following equation is obtained.

[Numerical formula 24]

$$G = (p_5 \cdot p_4 \cdot p_3 \cdot p_2)(p_1 \cdot g_0 + g_1) + \{(p_5 \cdot p_4)(p_3 \cdot g_2 + g_3) + (p_5 \cdot g_4 + g_5)\} \quad \cdots (29)$$

By studying the constitution of Equation (29) obtained above, one can see that a 6-bit CLA circuit having a constitution different from that of the circuit shown in Figure 8 can be formed using ~~said~~ the two types of gates (first and second logic gates) or three types of gates (first logic gate - third logic gate).--

Rewrite paragraph [0083] as follows:

--[0083] 4-bit CLA circuits 501-504 have 4-bit carry propagation signals and 4-bit carry generation signals output from 4-bit half adders 401-404 as inputs, and they output corresponding 1-bit carry propagation signals and 1-bit carry generation signals, respectively. That is, CLA circuit 501 takes carry propagation signal (p_0,..., p_3) and carry generation signal (g_0,..., g_3) of half adder 401 as its input; CLA circuit 502 takes carry propagation signal (p_4,..., p_7) and carry generation

signal ($g_4, \ldots, g_7$) of half adder 402 as its input; CLA circuit (503) takes carry propagation signal ($p_8, \ldots, p_{11}$) and carry generation signal ($g_8, \ldots, g_{11}$) of half adder 403 as its input; and CLA circuit 504 takes carry propagation signal ($p_{12}, \ldots, p_{15}$) and carry generation signal ($g_{12}, \ldots, g_{15}$) of half adder 404 as its input. Then, corresponding to the input, the 1-bit carry propagation signal shown in Equation (7) and the 1-bit carry generation signal shown in Equation (8) are calculated. As the result of calculation, CLA circuit 501 outputs carry propagation signal P_0 and carry generation signal G_0, CLA circuit 502 outputs carry propagation signal P_1 and carry generation signal G_1, CLA circuit 503 outputs carry propagation signal P_2 and carry generation signal G_2, and CLA circuit 504 outputs carry propagation signal P_3 and carry generation signal G_3. The 4-bit CLA circuits of this invention can be used as ~~said~~ the 4-bit CLA circuits 501-504. For example, the CLA circuit shown in Figure 1 and explained in Embodiment 1 can be used.--

Rewrite paragraph [0084] as follows:

--[0084] 2-bit CLA circuit 505 takes 2-bit carry propagation signal (P_0, P_1) and 2-bit carry generation signal (G_0, G_1) output from former-stage 4-bit CLA circuits 501 and 502 as input, and, corresponding to ~~said~~ the signals, outputs 1-bit carry propagation signal P_{1A} and 1-bit carry generation signal G_{1A}. Carry propagation signal P_{1A} and carry generation signal G_{1A} are expressed by the following equations.

[Numerical formula 25]

$$G_{1A} = P_1 \cdot G_0 + G_1 \quad \cdots (30)$$
$$P_{1A} = P_1 \cdot P_0 \quad \cdots (31)$$

--

Rewrite paragraph [0086] as follows:

--[0086] 3-bit CLA circuit 506 takes 3-bit carry propagation signals (P_0-P_2) and 3-bit carry generation signals (G_0-G_2) output from former-stage 4-bit CLA circuits 501-503 as inputs, and, corresponding to these inputs, outputs 1-bit carry propagation signal P_{2A} and 1-bit carry generation signal G_{2A}. Carry propagation signal P_{2A} and carry generation signal G_{2A} are expressed by the following equations.

[Numerical formula 26]

$$G_{2A} = P_2 \cdot P_1 \cdot G_0 + P_2 \cdot G_1 + G_2 \quad \cdots (32)$$
$$P_{2A} = P_2 \cdot P_1 \cdot P_0 \quad \cdots (33)$$

Here, for ~~said~~ the Equation (32), grouping and transformation are performed in the same way as for Equations (16), (19), (22) and (27). Grouping from the left side of Equation (23) leads to the following equation.

[Numerical formula 27]

$$G_{2A} = P_2 \cdot (P_1 \cdot G_0 + G_1) + G_2 \quad \cdots (34)$$

Grouping from the right side of Equation (23) leads to the following equation.

[Numerical formula 28]

$$G_{2A} = P_2 \cdot P_1 \cdot G_0 + \{P_2 \cdot G_1 + G_2\} \quad \cdots (35)$$ --

Rewrite paragraph [0087] as follows:

--[0087] 3-bit CLA circuit 506 corresponding to the constitution of Equation (34), for example, may have the constitution of the circuit shown in Figure 12(A). 3-bit CLA circuit 506 shown in Figure 12(A) has NAND gate 131, NOR gate 132, AND-NOR type composite gate 223, OR-NAND type composite gate 258, and inverters 323-325. Inverter 323 outputs NOT of carry propagation signal P_0. NAND gate 131 outputs NAND of carry propagation signals P_1 and P_2. NOR gate 132 outputs NOR of the output signals of inverter 323 and NAND gate 131. This output signal corresponds to the result of operation for carry propagation signal P_{2A} shown in Equation (33). AND-NOR type composite gate 223 outputs NOR of the AND of carry propagation signal P_1 and carry generation signal G_0 and the carry generation signal G_1. This output signal corresponds to NOT of the result of the operation of non-common item $(P_1 \cdot G_0 + G_1)$ in Equation (34). Inverter 324 outputs NOT of carry propagation signal P_2. Inverter 325 outputs NOT of carry generation signal G_2. OR-NAND type composite gate 258 outputs NAND of the OR of the output signals of AND-NOR type composite gate 223 and inverter 324 and the output signal of inverter 325. This output signal corresponds to the result of operation for carry generation signal G_{2A} shown in Equation (32). Also, 3-bit CLA circuit 506 corresponding to the constitution of Equation (35), for example, can be formed as the circuit shown in Figure 12(B). 3-bit CLA circuit 506 shown in Figure 12(B) has NAND gate 133, NOR gate 134, AND-NOR type composite gate 224, OR-NAND type composite gate 259, and inverters 326 and 327. Inverter 326 outputs NOT of carry propagation signal P_0. NAND gate 133 outputs NAND of carry propagation signals P_1 and P_2. NOR gate 134 outputs NOR of the output signals of inverter 326 and NAND gate 133. This output signal corresponds to the result of operation for carry propagation signal P_{2A} shown in Equation (33). AND-NOR type

composite gate 224 outputs NOR of the AND of carry propagation signal P_2 and carry generation signal G_1 and the carry generation signal G_2. This output signal corresponds to NOT of the result of operation for the group item $(P_2 \cdot G_1 + G_2)$ in Equation (35). Inverter 327 outputs NOT of carry generation signal G_0. OR-NAND type composite gate 259 outputs NAND of the OR of the output signals of NAND gate 133 and inverter 327 and the output signal of AND-NOR type composite gate 224. This output signal corresponds to the result of operation for carry generation signal G_{2A} shown in Equation (32). Both CLA circuits shown in FIGS. 12(A) and (B) are formed from ~~said~~ the first logic gate - third logic gate. That is, the CLA circuit shown in FIGURE 12(A) uses NAND gate 131 and NOR gate 132 as the first logic gate, AND-NOR type composite gate 223 and OR-NAND type composite gate 258 as the second logic gate, and inverters 323-325 as the third logic gate. The CLA circuit shown in Figure 12(B) uses NAND gate 133 and NOR gate 134 as the first logic gate, AND-NOR type composite gate 224 and OR-NAND type composite gate 259 as the second logic gate, and inverters 326 and 327 as the third logic gate. For example, the second logic gate may be realized with an AND-NOR type composite gate shown in Figure 2 or an OR-NAND type composite gate shown in Figure 3. Consequently, 3-bit CLA circuit 506 can have the circuit formed without using logic gates having 3 or more series stages of transistors inserted between the output terminal and power source line or ground line, such as a 3-input NAND gate, etc.--

Rewrite paragraph [0096] as follows:

--[0096] In the embodiments described above, CLA circuits for 3-6 bits and the adder using them have been explained. However, this invention is not limited to this scheme. One may form CLA circuits for any [number of] bits from two types of

logic gates (first logic gate, second logic gate) or three types of logic gates (first logic gate - third logic gate). For example, the least significant positions of the N-bit carry propagation signal ($p_{(N-1)}$ - p_0) and N-bit carry generation signal ($g_{(N-1)}$ - g_0) input to the CLA circuit are taken as the first position. AND of the various positions from the Nth position to kth position (where k is a natural number of 2-N) of the input carry propagation signal and the (k - 1)th position of the input carry generation signal is taken as the (k - 1)th logic operation item, and the Nth position of the input carry generation signal is taken as the Nth logic operation item. In this case, as shown in Equation (12), carry generation signal G output from the CLA circuit is obtained as a result of OR of the first logic operation item - Nth logic operation item. Also, as shown in Equation 13, carry propagation signal P output from the CLA circuit is obtained as a result of the operation of AND of the various positions from the first position to the Nth position of the input carry propagation signal. For the OR operation formulas of N items of the first logic operation item to the Nth logic operation item set side-by-side in order (operation formula for carry generation signal G), the following transformation is performed to obtain a logic formula having a constitution corresponding to the CLA circuit of this invention. First of all, grouping is performed with OR of every two adjacent items taken as a group item sequentially from the side of the first logic operation item to the side of the Nth logic operation item. When a common item exists in the two grouped items, OR of the two items in the group item is transformed to AND of the common item and the non-common item. If the number of group items in the grouped OR operation formula is larger than 2, ~~said~~ the grouping and deformation are further performed repeatedly with respect to the group items set side-by-side corresponding to the numerical

order of the first logic operation item - Nth logic operation item in the grouped OR operation formula. By means of ~~said~~ the transformation, an OR operation formula composed of two group items (first logic formula) is obtained. ~~Said~~ The first logic gate takes 2-bit signals as input, and outputs AND, NAND, OR or NOR of the input 2-bit signals.--

Rewrite paragraph [0097] as follows:

--[0097] In the embodiments, examples have been described in which 2-input NAND gates and 2-input NOR gates are taken as the first logic gate. However, one may also use 2-input AND gates and 2-input OR gates. For any of ~~said~~ the gates used, as needed, by means of combination of the third logic gate and first logic gate, it is possible to calculate AND of a plural-bit input carry propagation signal that is needed for calculation of carry propagation signal P and calculation of the common item in the first logic formula. The input signals of the first logic gate include signals corresponding to AND, NAND, OR and NOR of plural-bit input carry propagation signals (such as the output signal of another first logic gate), as well as input carry propagation signals and input carry generation signals. Also, the output signal of the third logic gate may also be input. The second logic gate takes 3-bit signals as input, and it outputs a signal corresponding to OR or NOR of the AND of 2-bit signals among the input signals and other 1-bit signals, or it outputs a signal corresponding to AND or NAND of the OR of 2-bit signals among the input signals and other 1-bit signals.--